2.5-WATT AND 5-WATT INTERNALLY MATCHED GaAs FETs FOR 10.7-11.7 AND 14-14.5GHz BANDS

Madhu Avasarala and Ding-Yuan S. Day

Avantek Incorporated
Milpitas California

ABSTRACT

A new 7.2mm GaAs FET chip with high gain, power, efficiency and low thermal resistance has been developed. Internally matched packaged devices using one and two such FETs have been developed for the 10.7-11.7 and 14-14.5GHz bands. At 11.7GHz the 7.2mm and 14.4mm devices have achieved power gain, and power-added-efficiency of 35.3dBm, 8dB, 33% and 37.8dBm, 8.0dB and 31.5% respectively at the 1dB gain compression point. At 14.5GHz the results are 34dBm, 7dB, 25% and 37.0dBm, 6dB and 18.5% respectively at the 1dB gain compression point.

INTRODUCTION

In recent years there has been a rising demand for GaAs power FETs for microwave communication systems in the X and Ku bands. The common carrier line-of-sight communications at 11GHz and the commercial Ku band SATCOM uplink are of particular interest. For these applications amplifiers with high power, gain, efficiency reliability, low cost and small size are very desirable. Higher power GaAs FETs are realized by increasing gate periphery, optimizing the device material, geometry, and processing. As a consequence of increasing gate width, device impedances decrease thereby necessitating uniform and low loss matching as close to the FET chip as possible. This has lead to the use of internal matching techniques. This paper describes the device geometry, layout, fabrication, characterization, internal matching circuits, dc, rf, and thermal performance of such a device.

DEVICE MATERIAL SELECTION AND PATTERN

The high quality VPE material uses an in situ active/buffer growth technique. The buffer layer of 2um thickness is grown directly on a Cr doped HB sub-strate. The buffer layer doping concentration is less than 1E13 cm-3. The active layer is sulphur doped to 3E17 cm-3. The profile exhibits an active buffer layer interface of less than 200 Å for the first decade of doping change as measured by standard C-V profiling. The sharp profile and the high electron mobility in the epi layer combine to produce a gm of 130 mS/mm-a high value for a large device. A thick active layer combined with proper double recess etching anables good manufacturability without using an N^+ cap layer.

A high performance power MESFET design must consider all aspects of channel and layout design. For the channel design, the gate length, gate finger width, and the channel spacing are the critical parameters. A gate length of 0.5um was used to reduce the gate capacitance. A gate finger width of 60um was used as an optimal compromise between gain degradation for 18GHz operation due to gate finger losses and chip size for a given total gate width. A channel spacing of 6.5um was defined as optimum in order to create the channel recess etch with good yields. The channel recess was set at 3.5um to achieve good power FET reliability (1).

The pitch was set at 18.5um to achieve a desirable thermal resistance as calculated by an inhouse thermal program. The overall gate layout is made up of 12 cells each cell consisting of 10 fingers. This design permits the FET to operate beyond 15GHz. Fig. 1 shows a picture of the FET chip.

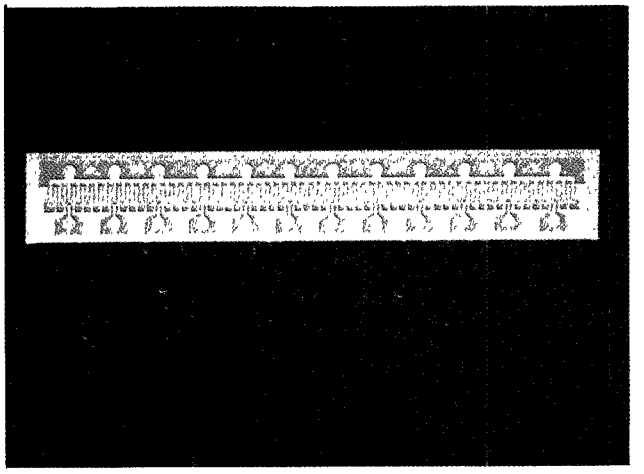

Figure 1 A 7.2mm GaAs FET

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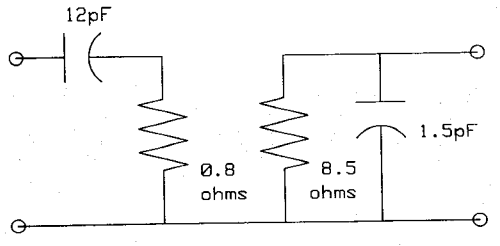
DEVICE FABRICATION

Device isolation is achieved via mesa etching using an isotropic wet etchant. The source and drain ohmic contacts use a standard AuGe-Ni-Au alloy process. The alloy cycle is kept short to achieve specific contact resistance less than 1E-6 ohm cm^2. The source and drain are then electrolytically plated to improve current handling. The channel recess is optimized to achieve a high breakdown voltage of BVgso 12v @ 1mA of Ig (2). The gate definition is done with contact photolithography. A 0.5um gate can be produced routinely. The evaporated Ti-Pt-Au metal system together with a tri-layer photoresist liftoff technique is used to produce the gate stripes. A plasma enhanced CVD dilicon nitride passivation layer is deposited over the active area to improve the reliability (3). Wraparound source grounding is used to minimize the common lead inductance. The source pads are interconnected through the chip sidewall to the backside metallization.

CHARACTERIZATION AND INTERNAL MATCHING

Special considerations are required due to the size of the device to feed the FET uniformly in magnitude/phase across the width in a 50ohm system. A prematched carrier was developed in which the input pre-match is a quarter wave transformer and the output match is provided by a 50 ohm tree network. These pre-matches were accurately modeled and de-embedding methods were used to translate measurements to the FET chip plane (4). S-parameters were used for small signal characterization. A semiautomatic loadpull system was used for large signal characterization (5). Using these broadband measurements simplified equivalent circuit models for the input and the output of the FET were obtained by computer optimization Fig. 2.



Simplified equivalent circuit for best power match for the 7.2 mm FET chip.

Figure 2 Simplified equivalent circuit for a 7.2mm FET.

Figs. 3, 4, 5 and 6 show the 7.2mm and the 14.4mm 10.7-11.7 and 14-14.5GHz internally matched devices. For the single chip case the input matching circuit consists of a 2 section quarter wave power divider. The input series capacitance of the FET is resonated by the input bond wire inductance. Due to the large width of the device it is extremely important to feed the chip uniformly in magnitude/phase and avoid any transverse resonances. This is achieved with a tree structure layout. The output matching network is synthesized via the Simplified Real Frequency Technique using lumped elements (6). These elements are converted to distributed form and the whole circuit reoptimized to create the final circuit. The input matching circuit uses a 0.254 mm thick alumina substrate. The low impedance lines are realized on a 0.1mm thick (Er=38) substrate. The output power combiner circuit uses a 0.381mm thick substrate. Thin film resistors are used in both the input and output divider/combiner circuts to achieve good isolation. The circuits are housed in a hermetic copper package. The package size excluding flange and leads is 11.93 x 10.67mm. The philosophy of design and layout for the 14.4mm devices is similar. The output of each FET is matched to 25 ohms, transformed to 100 ohms and then combined to give 50 ohms. The input of each FET is matched to 50 ohms, transformed to 100 ohms and combined to give 50 ohms. Such a design permits broadband operation beyond the typical commercial band requirements of 8%.

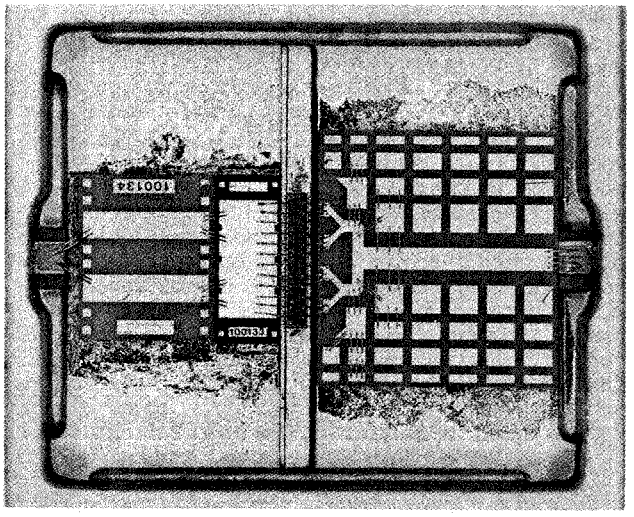


Figure 3 2.5-Watt Internal Matched FET (IMFET) for 10.7-11.7 GHz.

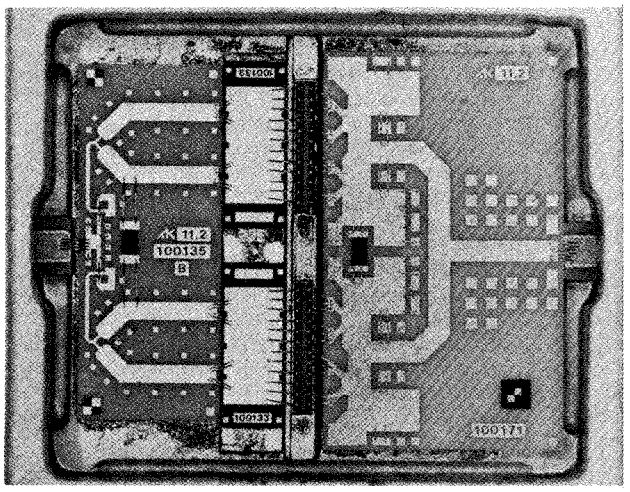


Figure 4 5-Watt 10.7-11.7 GHz IMFET.

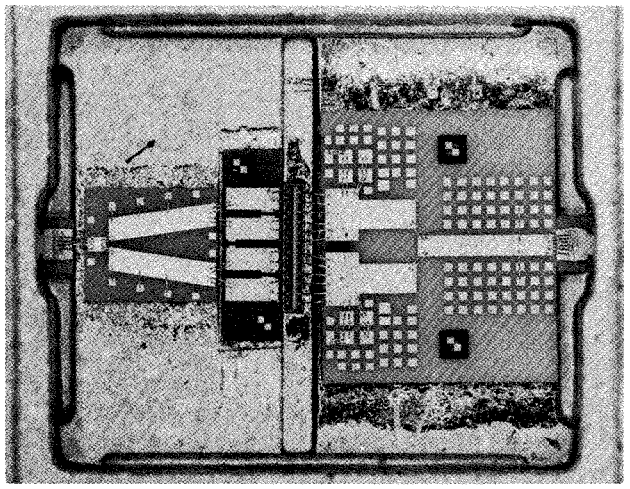


Figure 5 2.5-Watt 14.0-14.5 GHz IMFET.

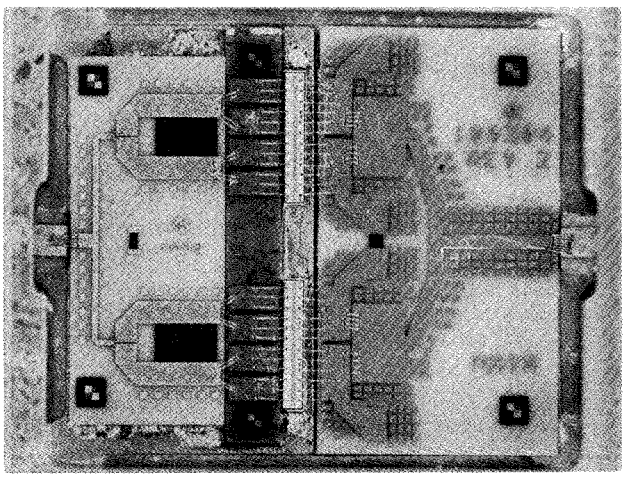


Figure 6 5-Watt 14.0-14.5 GHz IMFET.

D.C. CHARACTERISTICS AND R.F. PERFORMANCE

Fig. 7 shows the typical I-V characteristics. The devices are evaluated in a 50 ohm co-axial test fixture which consists of 50 ohm lines and a bias feed. No additional tuning is required. Figs. 8 and 9 show PldB and GldB vs. frequency and Pout vs. Pin for the 10.7-11.7 GHz devices. Figs 9 and 10 show corresponding information for the 14-14.5 GHz devices.

At 11.7 GHz the 7.2mm and the 14.4mm devices achieved power, gain, and a power added efficiency of 35.3dBm, 8dB, 33% and 37.8dBm, 8.0dB, and 31.5% respectively, at the 1dB gain compression point. At 14.5 GHz the results were 34dBm, 7dB, 25% and 37.0dBm, 6dB, and 18.5% respectively, at the 1dB gain compression point. These results reflect the best overall performance. The best performances for power, gain, or efficiency alone are much better. For example, the 7.2mm device at 14 GHz has achieved 36dBm with a gain of 7.5dB at the 1dB compression point.

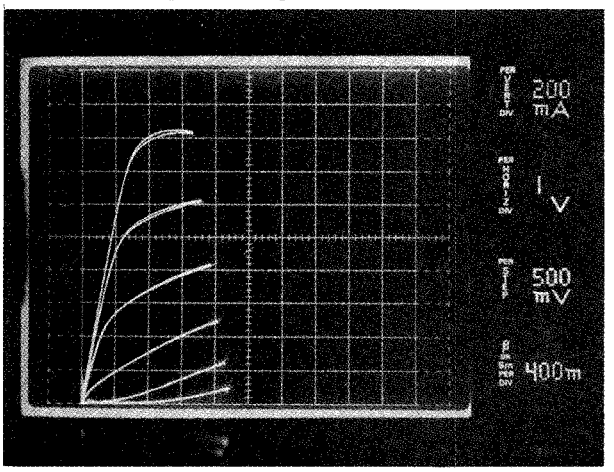


Figure 7 I-V characteristics for a typical 7.2mm FET.

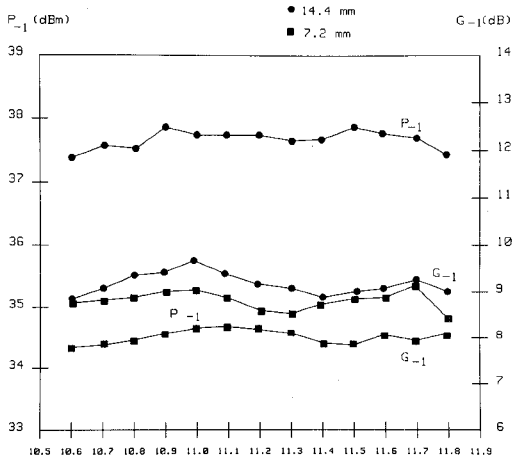


Figure 8 P-1 and G-1 vs. Frequency for 10.7-11.7 GHz IMFETs.

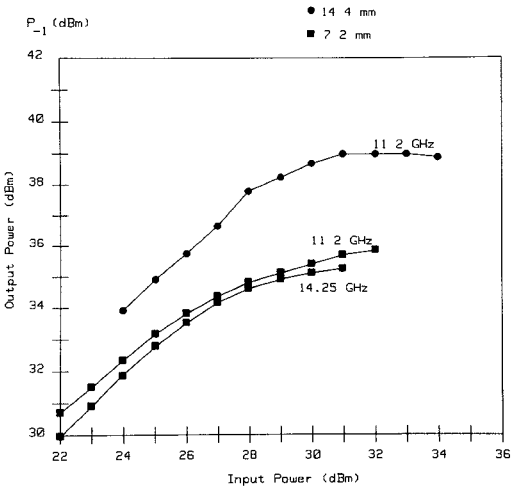


Figure 9 Pout vs. Pin for 10.7-11.7 GHz & 14.0-14.5 GHz IMFETs.

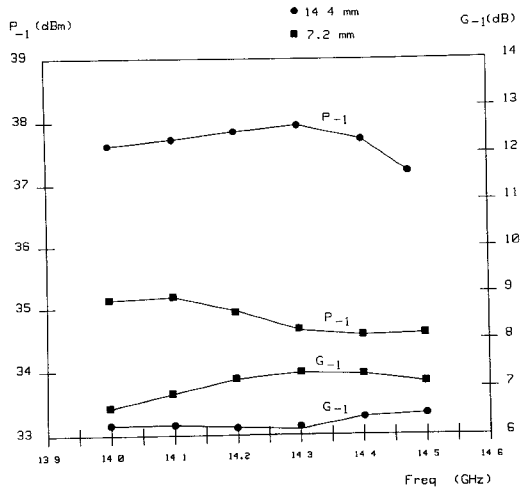


Figure 10 P-1 & G-1 vs. Frequency for 14.0-14.5 GHz IMFETs.

THERMAL PERFORMANCE

The thermal resistance channel-to-case at Tch=150 deg. C and Vds=9v was measured to be 10 deg. C/watt using an accurate and high resolution liquid crystal technique (7). The die thickness was .089mm. This will be reduced to .07mm to further decrease the Θjc to about 8.

CONCLUSION

A GaAs power FET with impressive performance in the X and Ku bands has been developed. To achieve these results the material, channel design and device layout have been optimized. Both channel and the gate recesses in addition to a wraparound source ground are used. The GaAs FETs were characterized using special circuit techniques to improve accuracy. Internally matched units were designed and fabricated using these GaAs FETs for Ku band applications. The internally matched units performance is excellent resulting in their use in TWT retrofit amplifiers and in Ku band uplink amplifiers in production quantities, attesting to the increasingly effective role played by power GaAs FETs in communications and radar applications.

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